Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) An interface circuit for process connections to computers, the interface circuit comprising:

at least one bidirectional input connection;

at least one bidirectional output connection, said bidirectional output connection ~~which is connected~~ connecting the interface circuit to a logic circuit by a galvanic decoupling device;

a plurality of switches~~, which can be controlled by signals,~~ whose inputs are connected directly or indirectly to said at least one bidirectional input connection and having a control pin for receiving first control signals;

~~several~~ a plurality of multiplexers whose inputs are connected to outputs of said switches and having control pins for receiving second control signals ~~which can be controlled by signals~~;

at least one analog comparator whose input is connected to an output of one of said plurality of multiplexers; and

at least one digital/analog converter whose input is connected to an output of one of said multiplexers;

wherein according to the state of one or more of the first and second signals which control the switches and multiplexers, the switches, multiplexers, analog comparators, and digital/analog converters ~~the components~~ are activated, deactivated, or changeable into different operating or switching states, with different analog or digital functions being assignable to the one or more bidirectional input connections.

2. Cancelled.

3. (Currently amended) The interface circuit of claim 1 wherein the multiplexers can be operated bidirectionally ~~, i.e.,~~ as multiplexers and as demultiplexers.

4. Cancelled.

5. (Original) The interface circuit of claim 1 wherein the one or more analog comparators are associated with a sample and hold circuit, whose input is connected to at least one input connection.

6. (Original) The interface circuit of claim 5 wherein the one or more analog/digital converters operate according to the principle of successive approximation.

7. (Original) The interface circuit of claim 1 wherein between the one or more input connections and one or more analog comparators, a current/voltage converter is connected, with the connection being switchable by the multiplexer.

8. (Original) The interface circuit of claim 1 wherein one or more of the analog comparators are connected after the controllable hysteresis circuit.

9. (Original) The interface circuit of claim 1 wherein a digital/analog converter is connected in the signal direction from the output connection to one or more input connections, with the connection being switchable in a controlled way by the multiplexer.

10. (Original) The interface circuit of claim 1 wherein at least two input connections are connected to each other over a measurement resistor and a controllable switch, with both connections of the measurement resistor being connected to a differential amplifier, whose output is connected to one or more analog/digital converters.

11. (Original) The interface circuit of claim 1 wherein several interface circuits are connected in a cascade arrangement and connected to the logic circuit.

12. Cancelled.

13. (Original) The interface circuit of claim 9 wherein several interface circuits are connected in a cascade arrangement and connected to the logic circuit.

14. (Currently amended) The interface circuit of claim 1 wherein [[a]] the galvanic decoupling device is connected between the interface circuit and the logic circuit.

15. (Currently amended) The interface circuit of claim 1 wherein [[an]] the galvanic decoupling device comprises an optocoupler ~~is connected between the interface circuit and the logic circuit~~.

16. (Original) The interface circuit of claim 1 wherein higher functions are implemented in the logic circuit, while only lower functions are implemented in the interface circuit.

17. (Original) The interface circuit of claim 16 wherein the higher functions comprise system functions.

18. (Original) The interface circuit of claim 16 wherein the logic circuit and the interface circuit are configured such that bidirectional serial communication takes place between these circuits.

19. (Original) The interface circuit of claim 17 wherein the logic circuit and the interface circuit are configured such that bidirectional serial communication takes place between these circuits.